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141 A vertically integrated VLSI design environment Jonathan Rosenberg, David Boyer, John Dallen, Stephen Daniel, Charles Poirier, John Poulton, Durward Rogers, Neil Weste

June 1983 Proceedings of the 20th conference on Design automation

Full text available: pdf(585.79 KB)

Additional Information: full citation, abstract, references, citings, index

A VLSI design system called VIVID is the heart of a newly developed, vertically integrated design environment. This environment provides support for all phases of design from highlevel system specification through on-site fabrication to construction of prototype systems. Key features already Implemented include: the use of a circuit description language at the level of a silicon assembler; a fast, highly interactive combination floor planner and layout editor; fast interactive timing simul ...

142 VLSI tools and architectures: Putting the new technology to work

John Ousterhout

January 1983 Proceedings of the 1983 computer science conference

Full text available: ndf(574.72 KG) Additional Information: full citation, abstract, references, index terms

This paper surveys the developments in VLSI that were triggered by the Mead-Conway design style. Computer-aided design tools and new architectures are reviewed, and future trends are suggested. The most significant future developments in tools are likely to center around the joining of procedural and graphical design methods, and the need for good routing aids. In the area of architecture, one of the most important unsolved problems is how to integrate special-purpose VLSI circuits easily i ...

143 How to assemble tree machines (Extended Abstract)

Sandeep N. Bhatt, Charles E. Leiserson

May 1982 Proceedings of the fourteenth annual ACM symposium on Theory of computing

Full text available: ndf(686.57 KB)

Additional Information: full citation, abstract, references, citings, index terms

Many researchers have proposed that ensembles of processing elements be organized as trees. This paper explores how large tree machines may be assembled efficiently from smaller components. A principal constraint that we consider is the limited number of external connections from an integrated circuit chip. We also explore the emerging

capability of restructurable VLSI which allows a chip to be customized after fabrication. We give a linear-area chip of m process	
144 Automated partitioning of hierarchically specified digital systems Thomas S. Payne, W. M. vanCleemput January 1982 Proceedings of the 19th conference on Design automation	
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Full text available: pdf(794.27 KB) Additional information, ide change, absences, temps, index terms	
This paper describes a heuristic algorithm for automatically partitioning digital systems. High level information contained within a hierarchical design is used to increase the effectiveness of this algorithm. This algorithm uses a constructive process to build a physical design of a hierarchically specified logic design. An iterative improvement step is then done.	
145 A minimum-impact routing algorithm	
Kenneth J. Supowit	(COLORDON
January 1982 Proceedings of the 19th conference on Design automation	
Full text available: pdf(895.70 K8) Additional Information: full citation, abstract, references, citings, index terms	
A routing heuristic is presented thatroutes two-terminal nets one at a time, for each net choosing the path so as to avoid adversely impacting the nets not yet routed. An algorithm is presented and proved to correctly implement this heuristic; the computational complexity of that algorithm is shown to be polynomially bounded, but perhaps still too great to be of practical use. Another, speedier algorithm is presented that seems to approximate the heuristic rather closely. Strong evidence is	
146 A symbolic design system for integrated circuits K. H. Keller, A. R. Newton, S. Ellis	
January 1982 Proceedings of the 19th conference on Design automation	
Full text available: pdf(828.20 KB) Additional Information: full citation, abstract, references, citings, index terms	
As integrated circuit design has become increasingly complex, the need for more effective data description techniques has become critical. Design verification from mask artwork data alone can consume vaste amounts of computer time for VLSI circuits, if it can be performed at all. The use of a symbolic design description, which allows the designer or synthesis program to express circuit structure as well as maintain full connectivity information, can reduce dramatically the burden plac	
147 Experiments using interactive color raster graphics for CAD Abe Shliferstein January 1982 Proceedings of the 19th conference on Design automation	
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Color raster graphics is being incorporated into CAD systems for printed circuit board (PCB) design. An interactive prototype CAD system developed as an experimental base is described, along with color graphics research using this prototype. Areas investigated included the generation and display of complex PCB's, the display of depth information using "2 1/2 dimensional" techniques, performance measurements on color raster systems, possibilities for new on-line design audit tech	
148 <u>Testing and Debugging Custom Integrated Circuits</u> Edward H. Frank, Robert F. Sproull December 1981 ACM Computing Surveys (CSUR) , Volume 13 Issue 4	

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149	Graphics language / one - IBM Corporate-Wide physical design data format David R. Lambert June 1981 Proceedings of the 18th conference on Design automation	
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	The evolution and structure of the IBM Corporate-Wide physical design data language, GL/1 (Graphics Language / One), is discussed. The need for a common graphics interface for communication among various design automation programs is demonstrated. At IBM, the same format is used from physical layout to mask generation for integrated circuit and printed circuit board designs.	
150	A parallel bit map processor architecture for DA algorithms	
	Tom Blank, Mark Stefik, Willem vanCleemput June 1981 Proceedings of the 18th conference on Design automation	
	Additional Information Still stating about to forward a picture index	
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	Bit maps have been used in many Design Automation (DA) algorithms such as printed circuit board (PCB) layout and integrated circuit (IC) design rule checking (DRC). The attraction of bit maps is that they provide a direct representation of two-dimensional images. The difficulty with large scale use of bit maps (e.g., for DRC on VLSI) is that the large amounts of data can consume impractical amounts of computation on sequential machines. This paper describes a processing architect	
151	Government interest and involvement in design automation development the VHSIC perspective Larry W. Sumney June 1981 Proceedings of the 18th conference on Design automation	
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	This paper describes the VHSIC Program and seeks to delineate the challenges for design automation which are vital to the Program's success. More than one-half of the VHSIC Program will focus on design architecture, software, and test. Because of the extreme importance of advanced militarized integrated circuits to our defense posture, alternatives to controlling the premature export of circuits, equipment, and technical data will be briefly reviewed. Finally, the opportunity to synergistic	
152	Structured machine design: An ongoing experiment	
	Richard F. Hobson May 1981 Proceedings of the 8th annual symposium on Computer Architecture	accessed.
	Additional Information, fivil abusing whether it references with the indext	
	ruii text available: pdi[6/2.55/N9]	
	In the following sections, the needs of structured architecture from the point of view of a single-user HLLCS is discussed. A prototype machine is introduced, and its design is treated as an ongoing experiment in structured machine design. This approach is relevant because historical evidence suggests that computer architecture (hardware and software) evolves slowly, requiring valuable information obtained through everyday use.	
153	The cube-connected cycles: a versatile network for parallel computation Franco P. Preparata, Jean Vuillemin	

Results (page 8): "interconnected cable" + "integrated circuits" + "emulation" + "circuits ... Page 3 of 5

Results (pa	age 8):	"interconnected	cable" +	"integrated	circuits" +	"emulation" +	"circuits	Page 4 of 5
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May 1981 Communications of the ACM, Volume 24 Issue 5

Full text available: pdf(996.20 KB)

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An interconnection pattern of processing elements, the cube-connected cycles (CCC), is introduced which can be used as a general purpose parallel processor. Because its design complies with present technological constraints, the CCC can also be used in the layout of many specialized large scale integrated circuits (VLSI). By combining the principles of parallelism and pipelining, the CCC can emulate the cube-connected machine and the shuffle-exchange network with no significant degradation ...

Keywords: Fourier transform, VLSI design, parallel processing, sorting

154	Detecting	bridging	and	stuck-al	faults	at inp	out and	l output	pins o	f standard	d digital
	componer										

Mark Karpovsky, Stephen Y.H. Su

June 1980 Proceedings of the 17th conference on Design automation

Full text available: pdf(904.10 KB)

Additional Information: full citation, abstract, references, citings, index

Due to the advances in the integrated circuit technology, there is an increasing importance in testing bridging (short circuit) failures in digital networks. Unfortunately, very little work has been done in this area. This paper presents the schemes for the detection of feedback bridgings between the inputs and outputs through the observation of oscillation and asynchronous behavior of sequential networks created by bridging faults. The lower and upper bounds on the number of tests for dete ...

155 An IC design station needs a high performance color graphic display

Neil Weste, Bryan Ackland

June 1980 Proceedings of the 17th conference on Design automation

Full text available: pdf(537,97 KB)

Additional Information: full citation, abstract, references, citings, index

Raster-scan color graphic displays provide increased visual feedback in many CAD areas. In addition the unique architecture of displays used for this purpose enable other CAD related problems to be solved within the hardware structure of the display. Achieving these features commensurate with human response times requires new architecures and algorithm development for color displays. This paper presents the architecture and some of the algorithms used in an advanced color display ...

156 Practical automated design of LSI for large computers

J Philip Singleton, Nigel R Crocker

June 1980 Proceedings of the 17th conference on Design automation

Full text available: ndf(361.53 KB) Additional Information: full citation, abstract, references, index terms

The design of large computers using LSI techniques requires relatively large numbers of different designs in relatively small quantities. The paper describes a system of designing integrated circuits rapidly and reliably in this environment using the Uncommitted Logic Array (Master Slice) approach. An integrated design, validation and production system has been developed from logical input to pattern generator tape production which takes away the need for knowledge of Silicon Layout techniq ...

157 The PUMA project: Computer design automation in the university

Ralph Grishman

January 1980 Proceedings of the ACM 1980 annual conference

Results (page 8): "interconnected cable" + "integrated circuits" + "emulation" + "circuits ... Page 5 of 5

Full text available: pdf(687.86 KB) Additional Information: full citation, abstract, references, citings, index

We shall describe in this paper a project in the New York University Computer Science Department which over the past few years has designed and built a series of high-speed scientific computer systems. These systems have been dubbed PUMA Computers (for Processing Unit with Microprogrammed Arithmetic). A major emphasis throughout this project has been on computer-aided design, manufacture, and testing.

158 The LASS hardware processor

Paul F. Kunz, Richard N. Fall, Michael F., Hanoch Brafman November 1978 Proceedings of the 11th annual workshop on Microprogramming

Full text available: pdf(591,25 KB) Additional Information: full citation, abstract, references, index terms

The problems of data analysis with hardware processors are reviewed and a description is given for a programmable processor. This processor, the 168/E, has been designed for use in the LASS multi-processor system; it has an execution speed comparable to that of the IBM 370/168 and uses the subset of IBM 370 instructions appropriate to the LASS analysis task.

159 Microprogrammed implementation of a single chip microprocessor

Skip Stritter, Nick Tredennick

November 1978 Proceedings of the 11th annual workshop on Microprogramming

Additional Information: full citation, abstract, references, citings, index Full text available: pdf(750,84 KB) terms

This paper considers microprogramming as a tool for implementing large scale integration, single-chip microprocessors. Design trade-offs for microprogrammed control are discussed in the context of semiconductor design constraints which limit the size, speed, complexity and pin-out of circuits. Aspects of the control unit of a new generation microprocessor, which has a two level microprogrammed structure, are presented.

160 A color graphics system for I.C. mask design and analysis

N. Weste

June 1978 Proceedings of the 15th conference on Design automation

Additional Information: full citation, abstract, references, citings, index Full text available: pd((690,67 KB) terms

In view of the continuing requirement for good interactive tools in the area of computer aided design, an advanced high-resolution monochrome and color, mini-computer controlled, graphics display has been designed and built. Considering the particular area of integrated circuit mask design, the ability to produce filled, color coordinated shapes extends the designer's interpretation of displayed layouts to a level not previously available with conventional graphics displays. Apart from this ...

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